

HD74AC195

4-bit Parallel-Access Shift Register

REJ03D0260-0200Z
(Previous ADE-205-380 (Z))
Rev.2.00
Jul.16.2004

Description

This shift register features parallel inputs, parallel outputs, J- \bar{K} serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; Shift from Q₀ towards Q₃.

Parallel loading is accomplished by applying the four bits of data, and taking the \bar{PE} Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the CP input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the \bar{PE} input is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs allow the first stage to perform as a J- \bar{K} or toggle flip-flop as shown in the function table.

Features

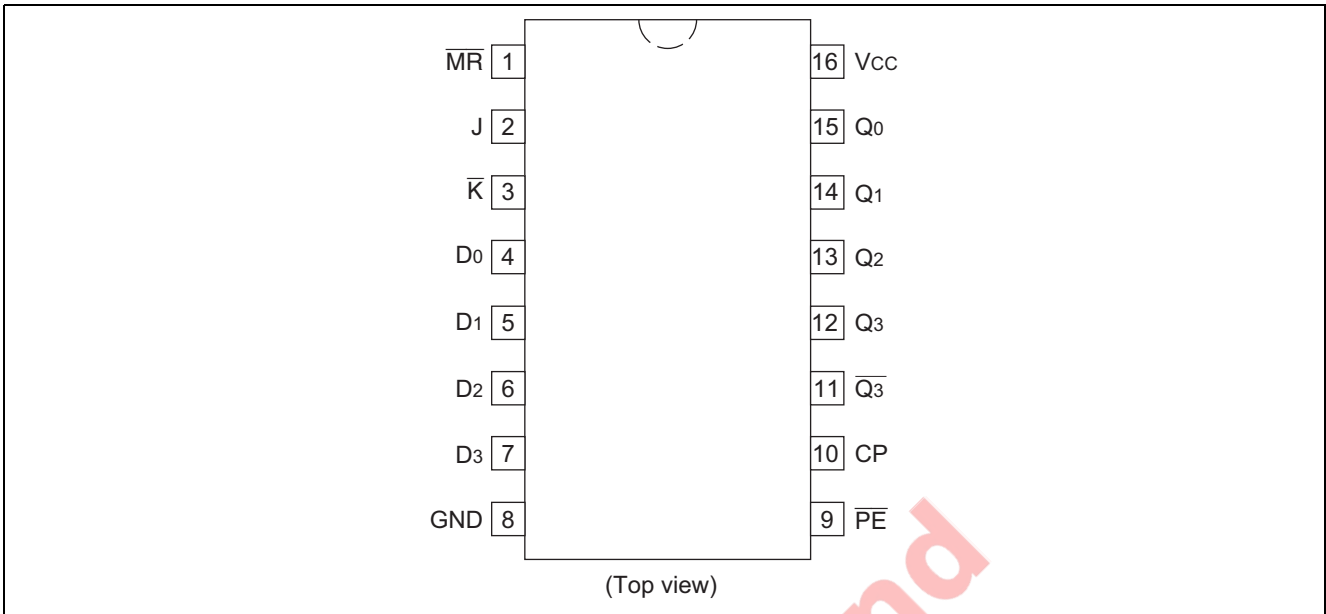
- Shift Right and Parallel Load Capability
- J- \bar{K} (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC195FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC195RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

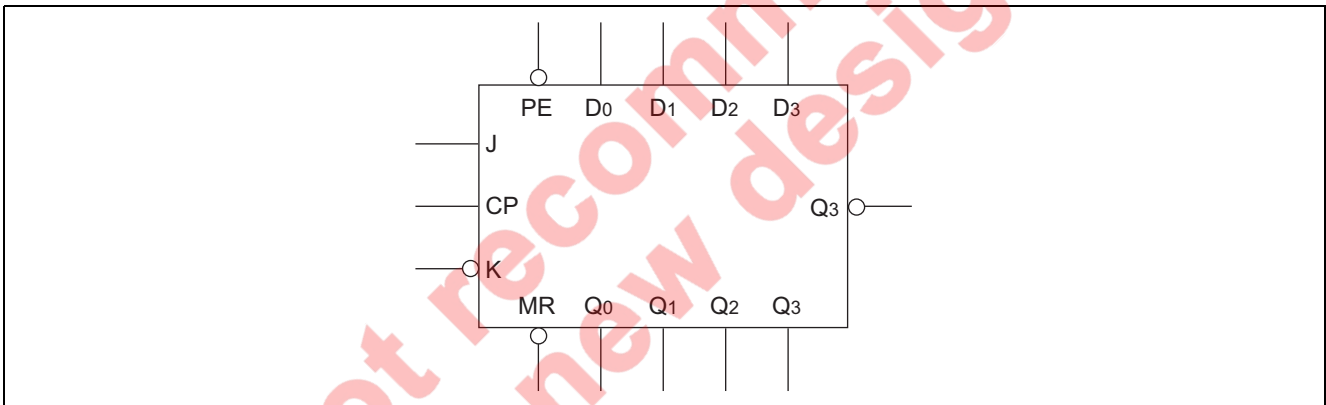
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



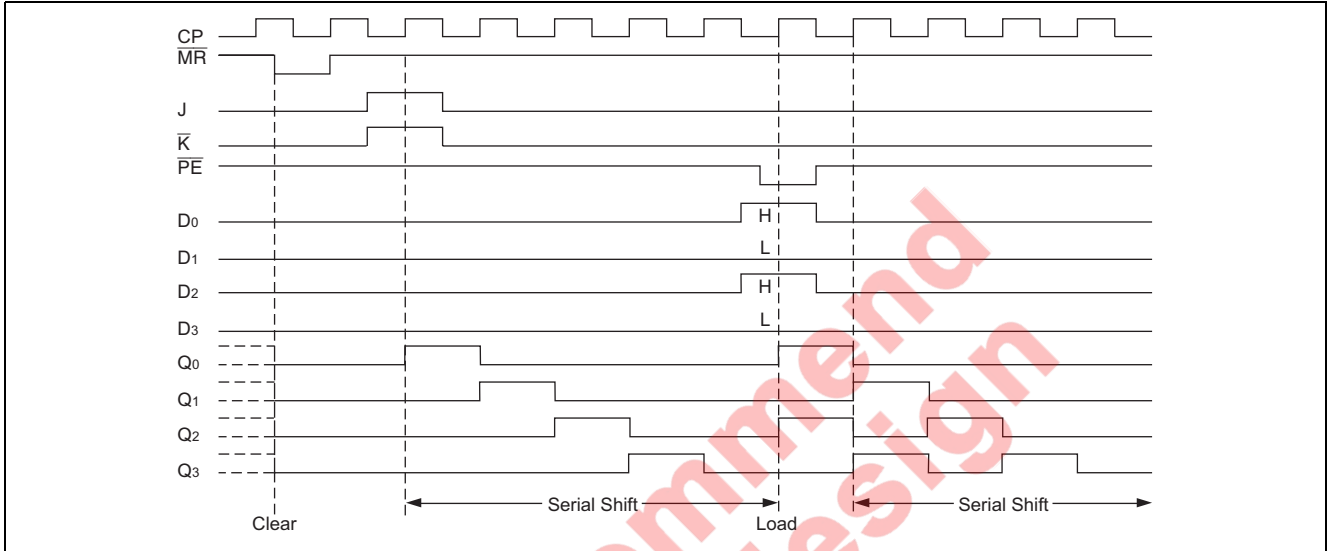
Logic Symbol



Pin Names

CP	Clock Pulse Input (Active Rising Edge)
D ₀ to D ₃	Parallel Data Inputs
\overline{PE}	Parallel Enable Input
\overline{MR}	Asynchronous Master Reset
J, \overline{K}	J- \overline{K} or D Type Serial Inputs
Q ₀ to Q ₃ , \overline{Q}_3	Outputs

Timing Diagram



Mode Select-Function Table

Operating Modes	Inputs						Outputs				
	\overline{MR}	CP	\overline{PE}	J	\overline{K}	D _n	Q ₀	Q ₁	Q ₂	Q ₃	\overline{Q}_3
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	\uparrow	H	H	H	X	H	q ₀	q ₁	q ₂	\overline{q}_2
Shift, Reset First Stage	H	\uparrow	H	L	L	X	L	q ₀	q ₁	q ₂	\overline{q}_2
Shift, Toggle First Stage	H	\uparrow	H	H	L	X	\overline{q}_0	q ₀	q ₁	q ₂	\overline{q}_2
Shift, Retain First Stage	H	\uparrow	H	L	H	X	q ₀	q ₀	q ₁	q ₂	\overline{q}_2
Parallel Load	H	\uparrow	L	X	X	d _n	d ₀	d ₁	d ₂	d ₃	\overline{d}_3

H : HIGH Voltage Level

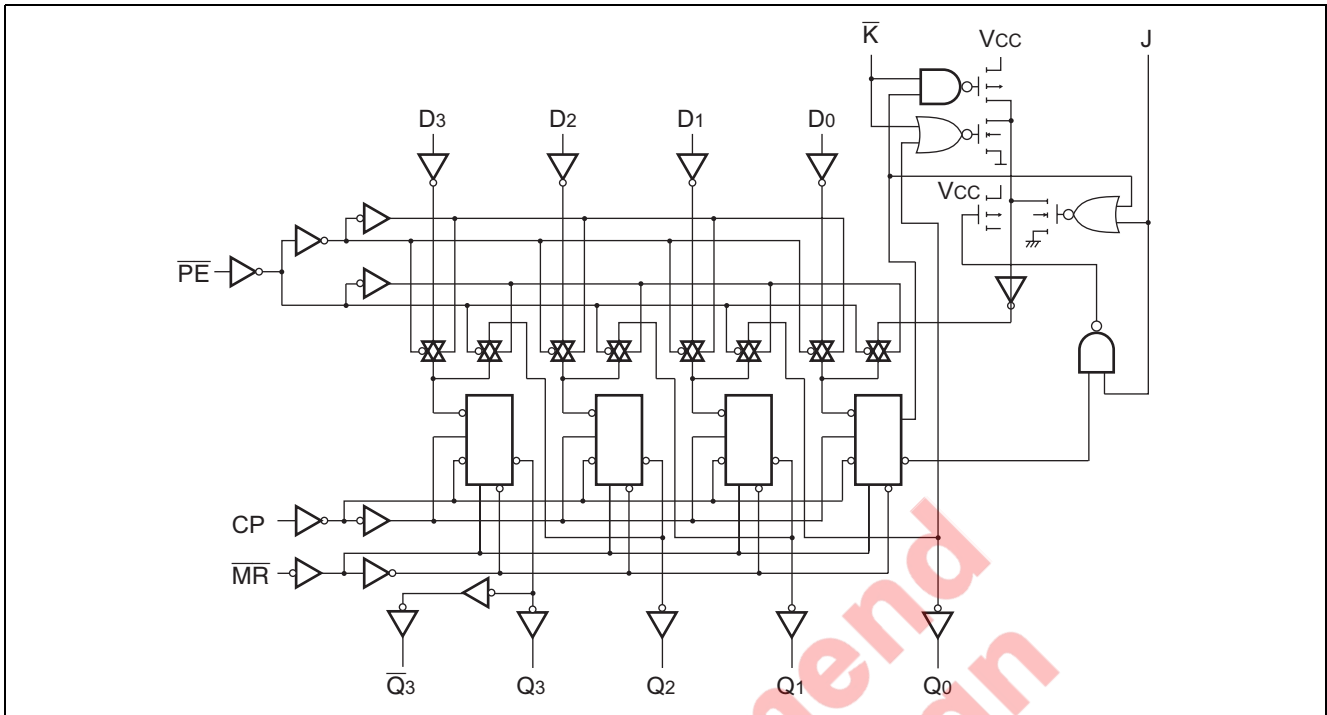
L : LOW Voltage Level

X : Immaterial

Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH transition.

\uparrow : LOW-to-HIGH clock transition.

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	$^{\circ}C$	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	t_r, t_f	8	ns/V	$V_{CC} = 3.0V$
				$V_{CC} = 4.5 V$
				$V_{CC} = 5.5 V$

DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition		
			min.	typ.	max.	min.	max.				
Input Voltage	V _{IH}	3.0	2.1	1.5	—	2.1	—	V	V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	3.15	2.25	—	3.15	—				
		5.5	3.85	2.75	—	3.85	—				
	V _{IL}	3.0	—	1.50	0.9	—	0.9		V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	—	2.25	1.35	—	1.35				
		5.5	—	2.75	1.65	—	1.65				
Output voltage	V _{OH}	3.0	2.9	2.99	—	2.9	—	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 μA		
		4.5	4.4	4.49	—	4.4	—				
		5.5	5.4	5.49	—	5.4	—				
		3.0	2.58	—	—	2.48	—			V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA	
		4.5	3.94	—	—	3.80	—				I _{OH} = -24 mA
		5.5	4.94	—	—	4.80	—				I _{OH} = -24 mA
	V _{OL}	3.0	—	0.002	0.1	—	0.1	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = 50 μA		
		4.5	—	0.001	0.1	—	0.1				
		5.5	—	0.001	0.1	—	0.1				
		3.0	—	—	0.32	—	0.37			V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA	
		4.5	—	—	0.32	—	0.37				I _{OL} = 24 mA
		5.5	—	—	0.32	—	0.37				I _{OL} = 24 mA
Input leakage current	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND		
Dynamic output current*	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} = 1.1 V		
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85 V		
Quiescent supply current	I _{CC}	5.5	—	—	8.0	—	80	μA	V _{IN} = V _{CC} or ground		

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	75	—	—	65	—	MHz
		5.0	100	—	—	85	—	
Propagation delay CP to Q _n or Q ₃	t _{PLH}	3.3	1.0	9.0	13.0	1.0	15.0	ns
		5.0	1.0	5.5	10.0	1.0	11.5	
Propagation delay CP to Q _n or Q ₂	t _{PHL}	3.3	1.0	9.0	13.0	1.0	15.0	ns
		5.0	1.0	6.5	10.0	1.0	11.5	
Propagation delay MR to Q ₂	t _{PLH}	3.3	1.0	7.5	10.5	1.0	12.0	ns
		5.0	1.0	5.5	8.0	1.0	9.5	
Propagaion delay MR to Q _n	t _{PHL}	3.3	1.0	6.0	9.0	1.0	10.5	ns
		5.0	1.0	5.0	7.0	1.0	8.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW J, \bar{K} or \bar{D}_n to CP	t _{SU}	3.3	3.0	5.5	7.0	ns
		5.0	2.0	4.0	5.0	
Hold time, HIGH or LOW J, \bar{K} or \bar{D}_n to CP	t _H	3.3	-0.5	2.0	3.5	ns
		5.0	0.5	1.5	2.0	
Setup time, HIGH or LOW $\bar{P}\bar{E}$ to CP	t _{SU}	3.3	3.5	5.0	7.0	ns
		5.0	2.5	4.0	5.0	
Hold time, HIGH or LOW $\bar{P}\bar{E}$ to CP	t _H	3.3	-2.0	0.0	0.0	ns
		5.0	-1.5	0.0	0.0	
Recovery time $\bar{M}\bar{R}$ to CP	t _{REC}	3.3	-1.5	0.5	0.5	ns
		5.0	-1.0	0.5	0.5	
Pulse width	t _w	3.3	-3.0	5.5	7.0	ns
		5.0	-3.0	4.5	5.0	

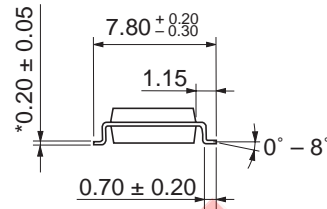
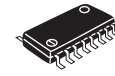
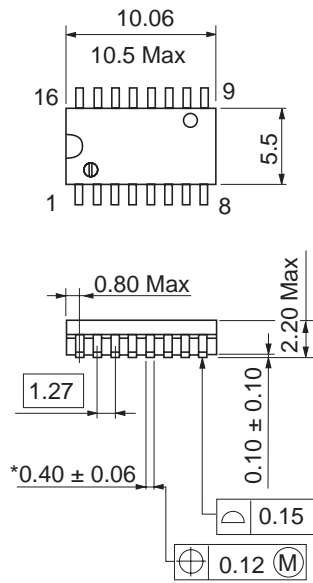
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	125	pF	V _{CC} = 5.0 V

Package Dimensions

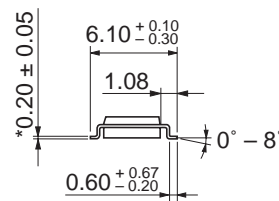
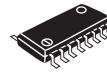
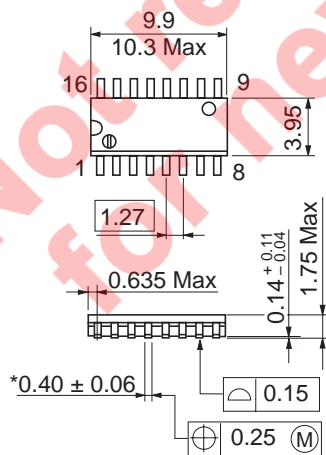
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

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